Remarks

Claims 1-10 are pending in the subject application and currently stand rejected. Favorable reconsideration of the pending claims is respectfully requested in view of the following remarks.

Applicant wishes to thank the Examiner for the courtesy extended to Sarah J. Knight during the telephonic conferences regarding the previous Office Action and the English translation of the Fukuzumi reference, which resulted in the previous Office Action being vacated and the present Action being mailed April 6, 2009. Examiner's remarks at page 2 and page 9 of the present Action constitute a summary of those telephonic conferences.

Claims 1, 2, 4-7 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Cloud *et al.* (U.S. 2002/0015322) in view of Lee *et al.* (U.S. 2001/0005604) and Noble *et al.* (U.S. 2002/0024083). Applicant respectfully traverses.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Indeed, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Furthermore, it is well established law that, "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." MPEP § 2143.01, citing, *In re* Ratti, 270 F.2d 810 (C.C.P.A. 1959).

Here, the Action at pages 4-5 states (regarding claim 1):

> Cloud *et al.* teach:
> a second contact plug 230 in insulating layer 232 ([0030]) and connected to the upper electrode 212;
> an anti-fuse (capacitor dielectric 222) ([0030]) . . . formed on the second contact plug in a second via hole, i.e., via hole in a "subsequent layer" containing capacitor 220, which would have been obviously insulating within the context of aforementioned multi-layered DRAM design; ... ; the third contact plug here being the concave central portion of top plate 223, filling the second via hole and formed within the anti-fuse, wherein the third contact plug does not directly contact any underlying insulating layer other than said anti-fuse; and
> a second metal wiring (top and side portions of top plate 213) formed on the insulating layer 232 and electrically connected to the third contact plug (through contiguous connection) and to the anti-fuse (which it abuts and hence exerts capacitive coupling thereon).

> **Cloud *et al.* do not specifically teach the limitation that the second contact plug is formed in a second insulating layer** because as we have seen Cloud *et al.* only provide an incomplete teaching of the bitline interconnect. However, following the teaching of Lee *et al.* as referred to above, it would have been obvious to locate the capacitor well above and separated by interlayer dielectric from the bit lines, motivation being provided by said separation of functionally independent metal parts . . . the additional teaching by Lee *et al.* only ensures placing bitline metal on a lower interlayer dielectric than the capacitor."

As emphasized above, the Examiner admits that Cloud *et al.* do not teach that the second contact plug is formed in a second insulating layer, but indicates that it would be obvious to include a second insulating layer when placing the capacitor above the bitline interconnect in view of Lee *et al.* However, this modification still does not arrive at the invention as claimed. Specifically, the cited references fail to teach or suggest a second contact plug in the second insulating layer **and** an anti-fuse formed on the second contact plug in a second via hole of the second insulating layer **and** a third contact plug filling the second via hole. That is, even if the "second contact plug" **230** as taught by Cloud *et al.* is formed in a second insulating layer, there is no teaching or suggestion that the "antifuse" (capacitor dielectric 222) and the "third contact plug" (the concave central portion of top plate 223) are also formed in the second insulating layer. Indeed, the "second metal wiring" (top and side portions of top plate 213) prevents such a modification (same issue arises in Noble *et al.* because of its similar structure). Lee *et al.* does not cure this defect because the capacitor dielectric 132 and upper electrode 134 are formed in a third insulating layer (interlayer dielectric film 136) separate from the second dielectric layer (interlayer dielectric film 126) having the second contact plug (upper portion of 128).

Furthermore, the capacitor structure shown in Cloud *et al.* cannot reasonably be interpreted to be formed in a "via hole" because there would not exist a via hole/plug structure in an insulating layer that is formed on the capacitor structure. Specifically, the top plate 223, which extends across the page (see Fig. 2 of Cloud *et al.* and Fig. 8 of Noble *et al.*) precludes the notion that the capacitor structure is disposed in a via hole. Moreover, one of ordinary skill in the art would not be motivated to modify the conformably disposed top plate 223 to remove the side portions of the top plate from being positioned touching the capacitor dielectric 222 (and similarly to modify the bottom plate from having the interior walls) because such a modification would adversely affect the capacitance of the capacitor within the highly integrated DRAM cell. Accordingly, the capacitor dielectric (222) and

top plate (223) of Cloud *et al.* cannot reasonably fall within the scope of an anti-fuse and third contact plug being in a via hole as specified in claim 1.

A finding of obviousness is proper only when the prior art contains a suggestion or teaching of the claimed invention. Here, it is only the applicant's disclosure that provides such a teaching, and an applicant's disclosure cannot be used to reconstruct the prior art for a rejection under §103. This was specifically recognized by the CCPA in *In re Sponnoble*, 56 CCPA 823, 160 USPQ 237, 243 (1969). Accordingly, Applicant respectfully requests reconsideration and withdrawal of this rejection.

Claims 3, 8, and 9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Cloud *et al.* in view of Lee *et al.*, Noble *et al.*, and Yamauchi *et al.* (U.S. 2001/0045667). Applicant respectfully traverses.

As mentioned above, Cloud *et al.* in view of Lee *et al.* and Noble *et al.* fail to teach or suggest a second contact plug in the second insulating layer **and** an anti-fuse formed on the second contact plug in a second via hole of the second insulating layer **and** a third contact plug filling the second via hole. Therefore, there is no teaching or suggesting of forming such a structure. For example, at a minimum, the cited references fail to teach or suggest "successively depositing first and second metal layers on the second insulating layer including the second via hole" and "forming an anti-fuse on the second contact plug in the second via hole and a third contact plug within the anti-fuse **by planarizing the first and second metal layers with the second insulating layer**," as specified in claim 3.

The Action at page 4 states that "the methods of forming a plurality of via holes by patterning an insulation layer and forming a conductive layer and contact plug by planarizing metal layers have long been known and conventional in the art of making interconnects including vias, as shown, for instance, by Yamauchi *et al.* ... ."

However, it has been well established in the patent law that the mere fact that the purported prior art could have been modified or applied in some manner to yield an applicant's invention does not make the modification or application obvious unless "there was an apparent reason to combine the known elements in the fashion claimed" by the applicant. *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 550 U.S. 398 (2007). Furthermore, an applicant's invention is not "proved obvious merely by demonstrating that each of its elements was, independently, known in the (purported) prior

art." *Id.* In addition, "[i]f a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." MPEP § 2143.01, referencing, *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

Here, the structure taught by Cloud *et al.* cannot be formed by performing a planarization process, nor is there any reason to modify the structure in order to do so. Indeed, the capacitor element, including the top plate 223 extending as a line, as taught by Cloud *et al.* is clearly formed before forming the insulating layer that the capacitor element is disposed in. Further, it is only the contact plug (electrical contact 230) that is formed within a via after deposition and planarizing processes with respect to the "second insulating layer 232."

Accordingly, Applicant respectfully requests that this rejection also be withdrawn.

In view of the foregoing remarks, Applicant believes that the claims as currently pending are in condition for allowance, and such action is respectfully requested.

Applicant invites the Examiner to call the undersigned if clarification is needed on any of this response, or if the Examiner believes a telephonic interview would expedite the prosecution of the subject application to completion.

The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 or 1.17 as required by this paper to Deposit Account 19-0065.

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